REMARKS

Reconsideration of this application is respectfully requested. Claims 1, 4-6, 9, 12 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,389,738 to Piosenka, et al. (hereinafter "Piosenka") in view of U.S. Patent No. 4,353,056 to Tsikos.

In this Amendment, Claim 1 has been amended. No new matter has been added. No claims have been canceled.

Rejections under 35 U.S.C. § 103(a)

Applicant respectfully submits that claims 1, 4-6, 9, 12 and 13 include limitations not taught or suggested by Piosenka and Tsikos, either individually or in combination.

Claims 1, 4

Applicants respectfully assert that claim 1 is not unpatentable under 35 U.S.C. § 103(a). Independent claim 1, as amended, recites:

> A circuit comprising:
> a first capacitor formed with a dielectric including the dielectric encasing elements of the circuit;
> a detector to detect changes in the capacitance of the capacitor, wherein the capacitance changes due to removal of dielectric material;
> approximately parallel conductors located proximate to circuit elements to protect from tampering; and
> a comparator to compare a reference voltage with a voltage at a node of the first capacitor, wherein the reference voltage is a voltage at a node of a second capacitor.

(Emphasis Added). Piosenka and Tsikos, either individually or in combination, do not teach or suggest "a detector to detect changes in the

capacitance of the capacitor, wherein the capacitance changes due to removal of dielectric material".

Piosenka discloses mechanisms to protect an integrated circuit (IC) device from tampering. One mechanism is to use a heavy metal to form a lid on the IC package. (Piosenka, col. 2, lines 26-30). Another mechanism is to detect the removal of the lid from the IC package by sensing a break in the conduction path. (Piosenka, col. 2, lines 44-51). Yet another mechanism is to sense changes in capacitance or resistance due to drilling or milling operations conducted on the lid. (Piosenka, col. 3, lines 25-32). Piosenka is silent about using the removal of dielectric material to detect a change in capacitance or assert any signals.

Tsikos does not supply this missing element. Tsikos merely discloses a fingerprint sensor having a sensing surface for receiving a fingerprint and sensing means for sensing the finger print. Tsikos does not teach or suggest a detector to detect changes in the capacitance of the capacitor, wherein the capacitance changes due to removal of dielectric material, as claimed.

Thus, claim 1 is not obvious over the combination of Piosenka and Tsikos. Further, Piosenka and Tsikos, either individually or in combination, do not teach or suggest "a comparator to compare a reference voltage with a voltage at a node of the first capacitor, wherein the reference voltage is a voltage at a node of a second capacitor", as claimed.

Piosenka discloses comparators that compare a first capacitor voltage with a reference voltage provided by a zener diode or a constant current source through resistors, which is not equivalent to comparing a first capacitor voltage with a reference voltage at a node of a second capacitor as claimed. As acknowledged by

the Examiner, Piosenka does not teach or suggest comparing a reference voltage at a node of a second capacitor with a voltage at a node of the first capacitor.

Applicant respectfully submits that Tsikos does not supply this missing element. Tsikos discloses pressing a finger against a sensing surface made of an array of small capacitors, thus changing the capacitance and the voltage across the capacitors in accordance with the ridges and valleys of the finger skin. (Tsikos, abstract). The voltage across each capacitor is detected and fed to a threshold detector that compares the voltages to one or more built-in thresholds. (Col. 4, lines 32-34). Thus, Tsikos discloses comparing a voltage at a capacitor with a threshold built in a threshold detector, and does not teach or suggest comparing a reference voltage at a node of a second capacitor with a voltage at a node of the first capacitor.

As such, even if Piosenka and Tsikos were combined, such a combination would not teach or suggest comparing a voltage at a node of the first capacitor with a reference voltage at the node of a second capacitor.

Further, the combination of Piosenka and Tsikos is improper for several reasons. There is no motivation in either Piosenka or Tsikos that Piosenka's comparator be modified from comparing a voltage at a node of the first capacitor with a reference voltage provided by a zener diode or a constant current source to comparing the voltage at the node of the first capacitor with a reference voltage at the node of a second capacitor.

The Examiner states that the motivation to combine is found in the references:

> It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the method of comparators monitoring the voltage output of sensors and comparing them to the reference voltage as disclosed by Piosenka with the method of using capacitors to hold the reference voltage as disclosed by Tsikos <u>because such sensors are easy to manufacture</u>.

(Office Action, page 7) (emphasis added). However, this motivation is disclosed by Tsikos as the motivation to make finger print sensors, and not to combine the "method of comparators monitoring the voltage output of sensors and comparing them to the reference voltage as disclosed by Piosenka with the method of using capacitors to hold the reference voltage as disclosed by Tsikos", as stated by the Examiner. Thus, the combination of Piosenka and Tsikos is improper.

For the reasons stated above, independent claim 1 is not obvious over this combination. Given that claim 4 depends from and includes the limitations of claim 1, applicants submit that claim 4 is not obvious over the combination under 35 U.S.C. § 103(a).

Claims 5-6

Applicants respectfully assert that claim 5 is not unpatentable under 35 U.S.C. § 103(a). Independent claim 5 recites:

> A circuit comprising:
> a detector comprising a first capacitor formed from conductive elements arranged such that removal of dielectric material from the vicinity of the conductive elements results in assertion of a signal disabling one or more operations of the circuit, the conductive elements arranged approximately parallel and proximate to elements of the circuit to protect from tampering; and
> a comparator to compare a reference voltage with a voltage at a node of the first capacitor, wherein the reference voltage is a voltage at a node of a second capacitor.

(Emphasis Added). As discussed above, Piosenka and Tsikos, either individually or in combination, do not teach or suggest a circuit in which removal of dielectric material from the vicinity of the conductive elements results in assertion of a signal. Furthermore, as discussed above, Piosenka and Tsikos, either individually or in combination, do not teach or suggest a comparator to compare a reference

voltage with a voltage at a node of the first capacitor, wherein the reference voltage is a voltage at a node of a second capacitor.

For the reasons stated above, independent claim 5 is not obvious over this combination. Given that claim 6 depends from and includes the limitations of claim 5, applicants submit that claim 6 is not obvious over the combination under 35 U.S.C. § 103(a).

Claim 9

Applicants respectfully assert that claim 9 is not unpatentable under 35 U.S.C. § 103(a). Independent claim 9 recites:

> A computer system comprising:
> a processor coupled to a memory by way of a bus;
> the processor comprising a detector, the detector comprising a first capacitor formed from conductive elements arranged such that removal of dielectric material from the vicinity of the conductive elements results in assertion of a signal disabling one or more operations of the circuit, the conductive elements arranged approximately parallel and proximate to elements of the processor to protect from tampering; and a comparator to compare a reference voltage with a voltage at a node of the capacitor, wherein the reference voltage is a voltage at a node of a second capacitor.

(Emphasis Added). As discussed above, Piosenka and Tsikos, either individually or in combination, do not teach or suggest a circuit in which removal of dielectric material from the vicinity of the conductive elements results in assertion of a signal. Furthermore, as discussed above, Piosenka and Tsikos, either individually or in combination, do not teach or suggest a comparator to compare a reference voltage with a voltage at a node of the first capacitor, wherein the reference voltage is a voltage at a node of a second capacitor.

For the reasons stated above, independent claim 9 is not obvious over this combination.

Claims 12-13

Applicants respectfully assert that claim 12 is not unpatentable under 35 U.S.C. § 103(a). Independent claim 12 recites:

> A computer system comprising:
> a processor coupled to a memory by way of a bus;
> the processor comprising a detector, the detector comprising a first capacitor formed from conductive elements arranged such that removal of dielectric material from the vicinity of the conductive elements results in assertion of a signal disabling one or more operations of the circuit, the conductive elements arranged approximately parallel and proximate to elements of the processor to protect from tampering; and a comparator to compare a reference voltage with a voltage at a node of the capacitor, wherein the reference voltage is a voltage at a node of a second capacitor.

(Emphasis Added). As discussed above, Piosenka and Tsikos, either individually or in combination, do not teach or suggest a circuit in which removal of dielectric material from the vicinity of the conductive elements results in assertion of a signal. Furthermore, as discussed above, Piosenka and Tsikos, either individually or in combination, do not teach or suggest a comparator to compare a reference voltage with a voltage at a node of the first capacitor, wherein the reference voltage is a voltage at a node of a second capacitor.

For the reasons stated above, independent claim 12is not obvious over this combination. Given that claim 13 depends from and includes the limitations of claim 12, applicants submit that claim 13 is not obvious over the combination under 35 U.S.C. § 103(a).

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Tom Ferrill at (408) 720-8300.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 7.22.05

Thomas S. Ferrill
Reg. No. 42,532
Tel.:(408) 720-8300

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026